[See Signature Page for Information on Counsel for Plaintiffs]

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-00877 JR/HRL **PLAINTIFFS' CONSOLIDATED RESPONSIVE CLAIM CONSTRUCTION BRIEF** **[RELATED CASES]**
HTC CORPORATION, HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-00882 JF/HRL
BARCO N.V., a Belgian corporation, Plaintiff, v. TECHNOLOGY PROPERTIES LTD., PATRIOT SCIENTIFIC CORP., ALLIACENSE LTD., Defendants.	Case No. 5:08-cv-05398 JF/HRL

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I. INTRODUCTION

Declaratory relief plaintiffs Acer, HTC and Barco entities as shown on the caption page (collectively "Plaintiffs") submit this joint brief in support of their claim construction positions.

The four patents-in-suit, which share the same specification, are directed to features of a specialized microprocessor. According to the specification, the development of microprocessors was headed in the wrong direction by using conventional external reference signals to clock the central processing unit ("CPU") and by incorporating a growing number of transistors to handle longer and more complex instructions. The inventors, in contrast, aimed to optimize the performance-to-cost ratio by minimizing the number of transistors and instructions, and in particular by integrating various special components and features onto a single chip. In order to achieve this goal, the patents disclose and claim the following special features: (1) a free-running on-chip oscillator clocking the CPU at a frequency that varies based upon environmental parameters such that the CPU always operates at its maximum frequency possible; (2) an arithmetic logic unit ("ALU") directly coupled to a push down stack such that the need for resolving source and destination addresses in instructions is eliminated; and (3) fetching and supplying multiple instructions to the CPU in parallel during a single memory cycle via the instruction register without using a pre-fetch buffer.

These key concepts are incorporated into Plaintiffs' proposed constructions. TPL, on the other hand, seeks to improperly broaden the claims by ignoring or distorting these concepts. TPL's proposed constructions also ignore disclaimers and amendments it made during prosecution or reexamination to overcome the prior art cited by the PTO. While some of the disputed terms were previously construed by Judge Ward of the Eastern District of Texas in a June 15, 2007 order,[1] Judge Ward did not take into account these subsequent disclaimers and amendments made after his ruling. Plaintiffs' proposed constructions properly consider the impact these disclaimers and amendments have on the interpretation of the claims.

[1] *Tech. Props. Ltd., et al. v. Matsushita Elec. Indus. Co., et al.* (hereafter "*TPL v. Matsushita*"), Case No. 2:05-cv-494, attached to Declaration of Kyle Chen (hereafter "Chen Decl.,") as Ex. A (hereafter "Ward Order").

II. DISPUTED TERMS

A. "Ring oscillator" ('336, '148 and '890) and related phrases

1. "ring oscillator" (Joint Claim Construction Statement, or "JCCS," row 22)

The term "ring oscillator" is recited in the asserted claims of the '336, '148 (division of '336) and '890 patents. The parties' respective constructions for this term are set forth below:

Plaintiffs' Construction [JCCS 22]	**TPL's Construction**
An oscillator having a multiple, odd number of inversions arranged in a loop, **wherein the oscillator is: (1) non-controllable; and (2) variable based on the temperature, voltage, and process parameters**[2] **in the environment.**	An oscillator having a multiple, odd number of inversions arranged in a loop

Judge Ward previously construed "ring oscillator" as "an oscillator having a multiple, odd number of inversions arranged in a loop," which is incorporated into both parties' constructions. Ward Order (Chen Decl., Ex. A), p. 11. The additional language in Plaintiffs' proposed construction reflects subsequent disclaimers made by TPL during on-going reexamination to distinguish prior art. In particular, after Judge Ward's construction and after the dismissal of the Texas litigation, TPL argued to the PTO during the reexamination of the '148 patent (division of the '336 patent) that the claimed "ring oscillator" was distinguishable from a voltage-controlled oscillator ("VCO") disclosed in U.S. Patent No. 4,689,581 to Talbot (Chen Decl., Ex. B) (hereafter "Talbot") as follows:

> Continuing, the patent owner further argued that the reference of Talbot does not teach [sic] of a "ring oscillator." The patent owner discussed features of a ring oscillator, such as being ***non-controllable***, and being ***variable based on the environment***. The patent owner argued that ***these features distinguish over what Talbot teaches***.

Interview Summary, 2/12/08, Control No. 90/008,227 (emphasis added) (Chen Decl., Ex. C).

TPL's expert admitted that a VCO is "almost universally implemented as a ring oscillator." Oklobdzija Depo. 12/10/10 (Chen Decl., Ex. D) at 71:25-72:23. Hence, the **only** reason Talbot's VCO is not the claimed "ring oscillator" is because Talbot's VCO is **not** "non-controllable" and "variable based on the environment," as argued by TPL. Interview Summary, 2/12/08, Control

[2] Since TPL has admitted that "environment" means "parameters of temperature, voltage, and process," (*see* Opening Brief at 17), the phrase "the temperature, voltage, and process parameters" has been included in Plaintiffs' proposed construction for clarification purposes.

No. 90/008,227 (Chen Decl., Ex. C) ("these features distinguish over what Talbot teaches"); *see also* Amendment, 2/26/08 (Chen Decl., Ex. H) ("Talbot discusses a ***voltage-controlled oscillator (VCO) 12***, but does not teach or disclose a ring oscillator.") (emphasis added)

In light of TPL's arguments made to the PTO after Judge Ward's ruling, the claimed "ring oscillator" must be (1) "non-controllable," and (2) "variable based on the environment," and Judge Ward's construction should be modified to conform to those explicit arguments made by TPL.[3] The reason is that a court "cannot construe the claims to cover subject matter broader than that which the patentee itself regarded as comprising its invention and represented to the PTO." *Microsoft Corp.*, 357 F.3d at 1349; *see also Rheox, Inc. v. Entact, Inc.*, 276 F.3d 1319, 1325 (Fed. Cir. 2002) ("Explicit arguments made during prosecution to overcome prior art can lead to narrow claim interpretations because 'the public has a right to rely on such definitive statements made during prosecution.'") (citations omitted).

Plaintiffs' proposed additions to Judge Ward's construction are also consistent with the specification's explanation of how the claimed "ring oscillator" is supposed to improve CPU performance. The problem as stated by the patents is that the CPU must operate "over wide temperature ranges, wide voltage swings, and wide variations in semiconductor processing," each of which affects the CPU's maximum frequency possible by a factor of two to four. *See* '336, 16:44-53 (factor of two); 17:19-22 (factor of four).

The specification criticizes the prior art solution, i.e., clocking the CPU at a fixed "rated clock speed" substantially lower than the CPU's theoretical maximum frequency to accommodate changes in environmental parameters:

> Temperature, voltage, and process all affect transistor propagation delays. **Traditional CPU designs** are done so that with the worse case of the three parameters, the circuit will function at the rated clock speed. The result[s] are **designs that must be clocked a factor of two slower than their maximum theoretical performance**, so they will operate properly in worse case conditions.

'336, 16:47-53 (emphasis added).

[3] The '148 reexamination applies to all patents-in-suit as they share the same specification and recite the same "ring oscillator." *Microsoft Corp. v. Multi-Tech Sys., Inc.*, 357 F.3d 1340, 1350 (Fed. Cir. 2004) ("Any statement of the patentee in the prosecution of a ***related*** application as to the scope of the invention would be relevant to claim construction . . . .") (emphasis added).

To avoid artificially constraining the CPU's frequency, the specification proposes a "variable speed" CPU clock (rather than the traditional fixed speed clock) comprising an **on-chip** "ring oscillator" in a **single** embodiment. The goal is for the on-chip ring oscillator's frequency to vary its speed based on the environment such that it always clocks the CPU "at the maximum frequency possible, but never too fast." '336, 16:54-17: 2-10. To achieve this goal, the on-chip ring oscillator must track the CPU's "maximum frequency possible," which shifts over "wide temperature ranges, wide voltage swings, and wide variations in semiconductor processing." '336, 16:44-47. The specification asserts that the on-chip ring oscillator does indeed track the CPU's maximum frequency possible because the CPU and the **on-chip** ring oscillator are made from the same transistors on the same die. *See* '336, 17:2-10; *see also* '336, 16:63-67 ("The ring oscillator **430** is useful as a system clock . . . because its performance tracks the parameters which similarly affect all other transistors on the same silicon die [including those transistors on the CPU].") .

To clock the CPU at its maximum frequency possible, the on-chip ring oscillator must be "non-controllable" (or "free running,"[4] as admitted by TPL and the inventors) so that it can naturally adjust its frequency by a factor of two to four over "wide" changes in the temperature, voltage and process parameters in the environment. *See* TPL's 30(b)(6) admissions and the inventors' admissions as explained in n. 3; *see also* Opening Brief at 2 ("Decoupling the system clock from the I/O clock allowed . . . freeing the system clock, and thus the CPU . . . ").

TPL argues that because its "frequency is determined by the parameters of temperature, voltage and process," the ring oscillator is "controllable, at a minimum, by temperature and voltage." Opening Brief at 17. TPL's argument mischaracterizes the specification, which simply teaches that the temperature, voltage and process parameters affect the ring oscillator's frequency. Indeed, the specification teaches absolutely nothing about the ring oscillator being "controllable."

[4] TPL admits that the on-chip oscillator in the '336 patent is a "free running" clock in the deposition of co-inventor Moore, who was TPL's Rule 30(b)(6) witness in the prior E.D. Texas suit, *TPL v. Matsushita* (Case No. 2:05-cv-494). *See* TPL 30(b)(6) Depo. (Moore) 7/10/2007 at 75:17-23, 79:3-6, 82:25-83:5 (Chen Decl., Ex. E). Both Moore and Fish, the two inventors of the patents-in-suit, also admitted that the on-chip clock is "free running." *See, e.g.*, Moore Depo. 11/4/10 at 301:14-302:1 (Chen Decl., Ex. F); Fish Depo 6/25/07 at 29:4-7 (Chen Decl., Ex. G).

TPL's argument is also fatally undermined by its explicit disclaimer made to the PTO during reexamination that the claimed ring oscillator is "non-controllable" and "variable based on the environment." Hence, Plaintiffs' construction should be adopted.

2. "An entire ring oscillator variable speed system clock in said single integrated circuit" and parallel terms

The phrase, "an entire ring oscillator variable speed system clock in said single integrated circuit," appears in claim 1 of the '336 patent. Judge Ward's construction of this phrase is reflected in both parties' proposals below. However, only Plaintiffs' proposal takes into account the subsequent arguments TPL made to the PTO about the claimed oscillator to distinguish over prior art, which were not available to Judge Ward. The parties' respective constructions (with differences shown in boldface type and strikeouts) are set forth below:

Plaintiffs' Construction [JCCS 23]	**TPL's Construction**
An ring oscillator variable speed system clock that is located entirely on the same semiconductor substrate as the CPU and does not ~~directly~~ rely on a ~~command input~~ control signal or an external crystal/clock generator to generate a clock signal, **wherein the ring oscillator variable speed system clock is: (1) non-controllable; and (2) variable based on the temperature, voltage, and process parameters in the environment**	An ring oscillator variable speed system clock that is located entirely on the same semiconductor substrate as the CPU and does not **directly** rely on a **command input** control signal or an external crystal/clock generator to generate a clock signal

Two other similar phrases appear in claims 6 and 10 of the '336 patent. All parties have treated all three phrases together, and the parties' competing constructions have identical differences. Claim 6 recites "an entire oscillator disposed upon said integrated circuit substrate," and the parties have proposed the following constructions:

Plaintiffs' Construction [JCCS 19]	**TPL's Construction**
An oscillator that is located entirely on the same semiconductor substrate as the CPU and does not ~~directly~~ rely on a ~~command input~~ control signal or an external crystal/clock generator to generate a clock signal, **wherein the oscillator is: (1) non-controllable; and (2) variable based on the temperature, voltage, and process parameters in the environment**	An oscillator that is located entirely on the same semiconductor substrate as the CPU and does not **directly** rely on a **command input** control signal or an external crystal/clock generator to generate a clock signal

Finally, claim 10 recites "providing an entire variable speed clock disposed upon said integrated circuit substrate," and the parties have proposed the following constructions:

Plaintiffs' Construction [JCCS 28]	**TPL's Construction**
Providing a variable speed clock that is located entirely on the same semiconductor substrate as the CPU and does not ~~directly~~ rely on a ~~command input~~ control signal or an external crystal/clock generator to generate a clock signal, **wherein the variable speed clock is: (1) non-controllable; and (2) variable based on the temperature, voltage, and process parameters in the environment**	Providing a variable speed system clock that is located entirely on the same semiconductor substrate as the CPU and does not **directly** rely on a **command input** control signal or an external crystal/clock generator to generate a clock signal

The Court should adopt Plaintiffs' language because it makes clear that the oscillator is "(1) non-controllable (or "free running," as admitted by TPL and the inventors (*see* n. 3)); and (2) variable based on the temperature, voltage, and process parameters in the environment," the same requirement that Plaintiffs propose be incorporated into the definition of "ring oscillator" as explained above. The inclusion of this language is supported by the subsequent reexamination file history and consistent with the sole embodiment described in the specification.

The remaining disputes are whether the claimed oscillator "does not rely" (Plaintiffs' proposal) or "does not ***directly*** rely" (TPL's) on a ***command input*** control signal or an external crystal/clock generator. As to these questions, Plaintiffs' proposal should be adopted.

TPL relies exclusively on Judge Ward's claim construction order[5] to support its proposal, but that impermissibly ignores the explicit disclaimers subsequently made, as discussed above. By

[5] In the prior litigation before Judge Ward, the accused infringers "argue[d] that the applicant disclaimed use of a control signal . . . to distinguish over prior art," while TPL "contend[ed] that it did not disclaim all types of control signals, such as voltage and current controlled oscillators; there was only a disclaimer of the more narrow 'command input.'" Ward Order (Chen Decl., Ex. A), pp. 11-12. Judge Ward resolved the dispute by holding:

> ***The Court agrees with the defendants that the applicant disclaimed the use of an input control signal and an external crystal/clock generator to generate a clock signal.*** Accordingly, the Court construes the term to mean "a ring oscillator variable speed system clock that is located entirely on the same semiconductor substrate as the CPU and ***does not directly rely on a command input control signal or an external crystal/clock generator*** to generate a clock signal."

Id. Although Judge Ward's prior order required that the oscillator not directly rely on a "command input" control signal, that must be changed in light of TPL's subsequent disclaimers during reexamination. TPL argued to Judge Ward that it "did not disclaim all types of control signals, such as voltage and current controlled oscillators," but later explicitly disclaimed all types of control signals to the PTO by distinguishing Talbot's voltage controlled oscillator. *Id.* Hence, all control signals should now be excluded.

arguing to the PTO that the claimed oscillator in the patents-in-suit is "non-controllable," TPL admitted that the claimed oscillator does not rely at all on ***any*** control signal. Logically, a "non-controllable" oscillator cannot rely in any way – directly, indirectly, or otherwise – on any "control signal"—including but not limited to "command input" control signals. Indeed, the specification does not disclose any "control signal" for the claimed oscillator. Therefore, TPL's proposal that the oscillator "does not ***directly*** rely on a ***command input*** control signal" must be rejected.

TPL's proposal is also an improper attempt to recapture the surrendered subject matter. As noted above, during reexamination, TPL distinguished the "non-controllable" and "variable based on the environment" ring oscillator from Talbot's "***voltage-controlled*** oscillator (VCO)" **12** in a "phase locked loop" **4**. *See* Amendment, 2/26/08 (Chen Decl., Ex. H) and Interview Summary, 2/12/08, Control No. 90/008,227 (Chen Decl., Ex. C); *see also* Talbot (Chen Decl., Ex. B), entitled "Integrated Circuit Phase Locked Loop Timing Apparatus," 3:5-7 ("The basic structure of the control loop circuit of the timing apparatus **4** is apparent from **FIG. 1** [reproduced below] and it will be seen that it is constituted by a **phase locked loop**.") (emphasis added).

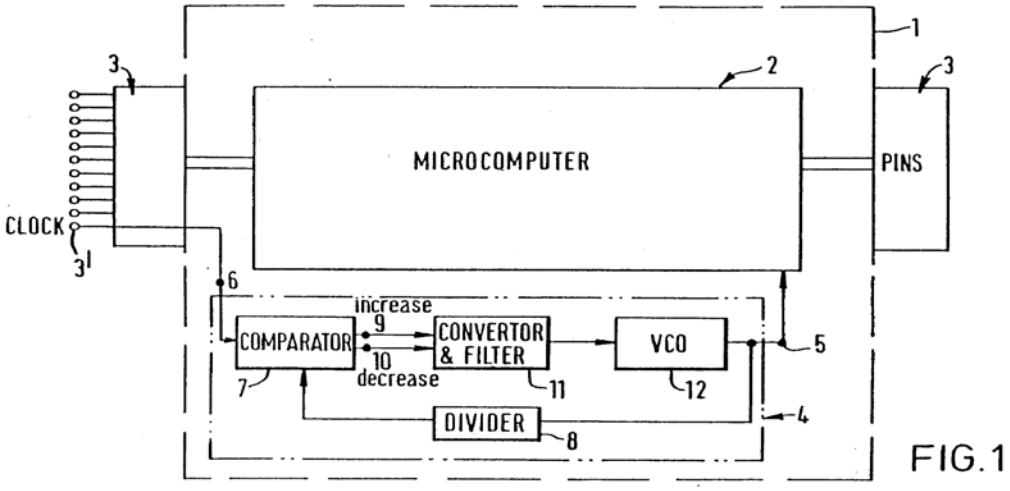


FIG. 1

In particular, Talbot discloses that the frequency of the VCO **12** is "controlled" by an external reference signal from the clock **3'**. *See* Talbot (Chen Decl., Ex. B), 2:58-63 ("The integrated circuit device of **FIG. 1** also includes timing apparatus, generally indicated by the reference numeral **4**, arranged to receive an ***external clock signal*** applied to one of the pins **3'** and to generate a timing signal at an output **5** for application to the logic device **2**.") (emphasis added). That external clock signal is supplied to a "comparator **7**" and, in conjunction with the "convertor

& filter **11**," produces a voltage control signal that "controls" the frequency of the VCO **12** based upon the external clock's frequency. Talbot (Chen Decl., Ex. B), 3:7-16, 3:26-36 ("[A] convertor and filter circuit **11** . . . is arranged to convert the output pulses from the comparator **7** into **a voltage signal for *controlling* the frequency of oscillation of a *voltage controlled* oscillator circuit 12**.") (emphasis added).

TPL's disclaimer of Talbot's VCO in fact disclaimed any ring oscillator that is controlled by a reference signal (as in a phase locked loop) or by a control signal (voltage, current or otherwise), as explained below. TPL's expert admitted that a VCO is "almost universally implemented as a ring oscillator," and that the phase locked loop "will try to have that ring oscillator run close to that reference." Oklobdzija Depo. 12/10/10 (Chen Decl., Ex. D) at 71:25-72:23. TPL's expert also admitted that a VCO "could be controlled by **voltage** or **current**." *See* Oklobdzija Depo. 12/22/2010 (Chen Decl., Ex. I) at 354:14-19 (emphasis added). Hence, the **actual** reason Talbot's VCO is not the claimed "ring oscillator" is because Talbot's VCO is **not** "non-controllable" or "variable based on the environment," as explicitly argued by TPL to the PTO. *See* Interview Summary, 2/12/08, Control No. 90/008,227 (Chen Decl., Ex. C). Instead, Talbot's VCO is "controlled" by a reference clock signal and a control signal, unlike the claimed "ring oscillator." *See* Talbot (Chen Decl., Ex. B), 3:5-36.

Contrary to TPL's disclaimer, TPL's infringement contentions explicitly accuse the "VCO" of a phase-locked loop as meeting the "ring oscillator" related elements. *See*, e.g., TPL's Infringement Contentions (4/30/2010) (Chen Decl., Ex. J). TPL apparently intends to argue that Judge Ward's construction is broad enough to include the VCO of a phase-locked loop as disclosed in Talbot. To that end, TPL's expert has taken the position that the VCO of a phase-locked loop is only "indirectly" controlled by the external reference clock signal. *See* Oklobdzija Depo. 12/22/2010 (Chen Decl., Ex. I) at 356:13-18.

In light of TPL's disclaimers made subsequently to Judge Ward's order, the on-chip oscillator or clock in the claimed invention does not rely on any "control signal or an external crystal/clock generator," either directly, indirectly, or otherwise. Hence, the words "directly" and "command input" should be removed, and Plaintiffs' proposal should be adopted in its entirety.

3. "Clocking said CPU"

This phrase, "clocking said CPU," appears in all asserted independent claims of the '336 patent. The parties' proposed constructions are set forth below.

Plaintiffs' Construction [JCCS 20]	**TPL's Construction**
Timing the operation of the CPU[6] **such that it will always execute at the maximum frequency possible, but never too fast**	Timing the operation of the CPU

Plaintiffs' proposed construction of "clocking said CPU" includes a limitation—that the CPU "will always execute at the maximum frequency possible, but never too fast"—based on the specification and patent owner's disavowal of claim scope during prosecution. The '336 patent teaches only ***one*** embodiment in which: "By deriving system timing from the ring oscillator **430**, CPU **70** will always execute at the maximum frequency possible, but never too fast." '336, 16:59-17: 2. The specification describes this feature as an advancement over "[t]raditional CPU designs," criticized as constraining the CPUs to "a factor of two slower than their maximum theoretical performance" to account for "worse case conditions." '336 patent, 16:50-53.

Because the purported advantage of the **sole** embodiment of the clocking invention is disclosed to be a CPU executing at its maximum frequency possible, but never too fast, the claim term "clocking said CPU" is appropriately limited to that feature. "[W]hen the preferred embodiment is described in the specification as the invention itself, the claims are not necessarily entitled to a scope broader than that embodiment." *Edward Lifesciences LLC v. Cook Inc.*, 582 F.3d 1322, 1330 (Fed. Cir. 2009) (citation omitted). Moreover, where the description of the invention "describes a feature of the invention ... and criticizes other products ... that lack that same feature, this operates as a clear disavowal of these other products." *Id.* at 1333. The prosecution history further supports Plaintiffs' construction. During prosecution, the applicants relied upon this feature to distinguish U.S. Patent No. 4,670,837 to Sheets (Chen Decl., Ex. K) ("Sheets"), stating that Sheets lacked the following "aspect" of the claimed invention:

> [T]he plurality of transistors included within the ring oscillator clock have operating characteristics which vary similarly to operating characteristics of transistors included within the microprocessor, thereby enabling the processing

[6] Plaintiffs partially adopt TPL's construction ("timing the operation of the CPU") and condenses the additional language to focus and simplify the dispute.

> frequency of the microprocessor to track the speed of the ring oscillator clock: ***'...CPU 70 executes at the fastest speed possible using the adaptive ring counter clock 430.'***

Amendment, 4/15/96, pp. 8-9, Chen Decl., Ex. L (emphasis added).

Because the applicants made this explicit argument to overcome the Sheets reference, they have disavowed any claim scope that would include a CPU not clocked to always execute at the maximum frequency possible, but never too fast. *See Rheox, Inc.*, 276 F.3d at 1325. Hence, Plaintiffs' proposal should be adopted.

B. "External clock" ('336)

The term "external clock" appears as part of the larger phrase "off-chip external clock" in claims 6 and 10 of the '336 patent. The parties have proposed the following constructions:

Plaintiffs' Construction [JCCS 24]	**TPL's Construction**
A clock not on the central processing unit	A clock not on the integrated circuit substrate

TPL made amendments to the claims of the '336 patent during reexamination, which were not available at the time of Judge Ward's claim construction order. The amendments make clear that an external clock is "a clock not on the central processing unit," as Plaintiffs have proposed.

In order to overcome a prior art rejection based upon U.S. Patent No. 4,766,567 to Kato ("Kato") (Chen Decl., Ex. M), TPL acknowledged that the term "external clock" does not exclude an on-chip clock by amending claims 6 and 10 to add the phrase "off-chip" in front of "external clock." TPL argued that this amendment distinguished the '336 patent over Kato:

> Kato's clock 15 was cited in the final Office action as corresponding to the "external clock" recited in Claims 6 and 10. Kato shows in Fig. 1 and discloses in Col. 4, Lines 27-42, for example, that both clocks (14 & 15) are formed on the substrate (10) along with the data processing circuit:
>
> * * *
>
> Kato's clock 15 clearly is not off chip. Rather, Kato's clock (15) is on the same substrate (10) as the components of the data processing circuit. Kato therefore does not teach or even suggest "an off-chip external clock" as recited in Claims 6 and 10.

Amendment, 5/12/09, pp. 16-17 of 21, Chen Decl., Ex. N (underlining in original).

Based on this prosecution history, an "external clock" is not on the central processing unit, but may be on the same integrated circuit substrate (as in Kato). An "***off-chip*** external clock," on the other hand, is an external clock that is not on the integrated circuit substrate at all.

TPL's construction of "external clock" should be rejected because it renders the phrase "off-chip" without meaning and superfluous. *Becton, Dickinson & Co. v. Tyco Healthcare Grp., LP*, 616 F.3d 1249, 1256-57 (Fed. Cir. 2010) ("Claims must be 'interpreted with an eye toward giving effect to *all terms* in the claim.'") (citation omitted; emphasis added). "If the ['off-chip'] limitation . . . is not to be read out of the asserted claims, it must require an additional element beyond that which is already called for by the ['external'] limitation." *Id.* at 1257. Plaintiffs' proposed construction is the only one that gives meaning to all words in the phrase, "off-chip external clock."

Although the parties agree that the "***off-chip*** external clock" recited in claims 6 and 10 is "a clock not on the integrated circuit substrate," it is important that the Court construe the smaller term "external clock" because it has potentially significant implications on infringement and damages issues. Under the doctrine of intervening rights, if TPL substantively amended claims 6 and 10 during the reexamination of the '336 patent, TPL is only entitled to recover damages for alleged infringement occurring after the completion of the reexamination. *See* 35 U.S.C. §§ 252, 307(b). Accordingly, the Court should construe the phrase "external clock" to define the difference between the "***off-chip*** external clock" (amended) and the "external clock" (original).

C. "[Including a plurality of electronic devices] correspondingly constructed of the same process technology with corresponding manufacturing variations" ('336)

This phrase is recited in claim 1 of the '336 patent. The dispute concerns the meaning of the phrase "same process technology." The parties have proposed the following constructions:

Plaintiffs' Construction [JCCS 17]	**TPL's Construction**
Correspondingly constructed **with the same transistors on the same die under the same process parameters**[7] with corresponding manufacturing variations	Constructed **using the same manufacturing process technology** with corresponding manufacturing variations

Plaintiffs' construction of "the same process technology" is based on the teaching of the specification. The only teaching in the '336 patent respecting how the ring oscillator's frequency can be made to track the CPU's "maximum frequency possible" is that they are constructed with

[7] Plaintiffs have clarified their proposed construction based upon the intrinsic record to focus and simplify the dispute.

the same transistors on the same die under the same process parameters:

> For example, if the processing of a particular die is not good resulting in slow transistors, the latches and gates on the microprocessor **50** will operate slower than normal. Since the microprocessor **50**['s] ring oscillator **430** is made from ***the same transistors on the same die*** as the latches and gates [on the microprocessor **50** having the CPU], it too will operate slower (oscillating at a lower frequency), providing compensation which allows the rest of the chip's logic [including the CPU of microprocessor **50**] to operate properly.

'336, 17:2-10 (emphasis added).

TPL's proposed construction of "same process technology" simply adds the word "manufacturing," which does not construe "same process technology" at all, and instead merely rewrites the claim in a vague way that is unsupported by the specification. Nowhere does the specification use the term "manufacturing process technology," let alone define it. Hence, TPL's construction should be rejected, and Plaintiffs' construction should be adopted.

D. "Operates asynchronously to" ('336) and related terms

The phrase "operates asynchronously to" appears identically at the end of claims 11, 13 and 16 of the '336 patent added in the reexamination as part of the longer phrase: "wherein said central processing unit **operates asynchronously to** said input/output interface." The dispute turns on the meaning of "asynchronously." The parties' constructions are set forth below:

Plaintiffs' Construction [JCCS 29]	**TPL's Construction**
operates without a timing relationship to/with	timed by independent clock signals

The claimed microprocessor has a "variable speed" ring oscillator, as explained above, that clocks the CPU at its maximum frequency possible, which varies depending on the environment. However, for the microprocessor to communicate with outside components, "[t]he external world must be synchronized to the microprocessor **50** for operations such as video display updating and disc drive reading and writing." '336, 17:23-25.

To synchronize the microprocessor with the external world, a second, fixed speed clock for timing the I/O interface is provided. "This synchronization is performed by the I/O interface **432**, speed of which is controlled by a conventional crystal clock **434**." '336, 17:25-27.

The specification explains that this "dual clock scheme" has the additional advantage of not dragging down the CPU's speed with the typically slower I/O interface:

> Most microprocessors derive all system timing from a single clock. The disadvantage is that different parts of the system can slow all operations. The microprocessor **50** provides a dual-clock scheme as shown in **FIG. 17**, with ***the CPU 70 operating asynchronously to I/O interface 432*** forming part of memory controller **118** (FIG. 2) and the I/O interface **432** operating synchronously with the external world of memory and I/O devices. ***The CPU 70 executes at the fastest speed possible using the adaptive ring [oscillator] clock 430.***

'336, 17:12-21 (emphasis added).

To achieve the stated goal that the I/O interface not prevent the CPU from executing at the fastest speed possible, the fixed frequency clock for the I/O interface must "operate asynchronously," or "have no timing relationship with the CPU's variable speed ring oscillator clock." Indeed, it is logically impossible for the CPU's "***variable*** speed clock" to have any timing relationship with the I/O interface's ***fixed*** frequency clock.

Standard computer dictionaries also define an asynchronous operation as "an operation that proceeds independently of any timing mechanism, such as a clock." *Microsoft Press Computer Dictionary* 24 (1991), Chen Decl., Ex. O. This definition is supported by the specification, which makes clear that the CPU must operate without a timing relationship with the I/O interface.

Contrary to the plain meaning of "asynchronous," TPL's construction appears to be calculated to include "independent" clock signals that nevertheless have a timing relationship or are, in fact, synchronized. A simple example of "independent" yet synchronized clocks comes from old war movies in which soldiers synchronize their "independent" wrist watches. During reexamination, to distinguish the Kato prior art as to claims 6 and 8, TPL similarly argued that "independent" clocks may be nonetheless synchronized under a section of its written response entitled "Synchronism Does Not Preclude Independence." *See* Amendment, 9/8/08, p. 21 of 28, Chen Decl., Ex. P.

TPL's admission to the PTO that two "independent" clocks can nonetheless operate "synchronously" fatally undermines its position on the meaning of "asynchronously." Construing the phrase "operates asynchronously to" to mean "timed by independent clock signals" would be impermissibly broad because, as admitted by TPL, such a construction would include both asynchronous and synchronous operations. Plaintiffs' proposal should therefore be adopted.

E. "Exchanging coupling control signals, addresses and data" ('336)

This phrase appears in claims 6 and 10 of the '336 patent, which recite "exchanging coupling control signals, addresses and data" between the I/O interface and the central processing unit. The dispute focuses on the meaning of "exchanging." The parties' constructions are below:

Plaintiffs' Construction [JCCS 18]	**TPL's Construction**
Transmitting ***and*** receiving coupling control signals, addresses, and data	Transmitting ***and/or*** receiving coupling control signals, and addresses, and data

Plaintiffs' construction is consistent with the intrinsic record and the plain and ordinary meaning of "exchanging," which requires ***both*** the transmission and receipt of information. The dictionary definition of "exchange" is "[t]o take or give in return for something else," *Webster's II New College Dictionary* at 390 (1995) (Chen Decl., Ex. Q), which clearly entails a ***two-way*** transaction. Two persons cannot be said to be "exchanging" business cards, for example, when only one person is giving her card to the other. TPL's attempt to cover unilateral transmission **or** receipt of information cannot be reconciled with the plain and ordinary meaning of "exchanging."

This meaning is confirmed by the intrinsic record, which describes a two-way exchange of information between the CPU and the I/O interface. As shown in Figure 17 of the '336 patent, "[r]ecoupling between the CPU **70** and the interface **432** is accomplished with handshake signals on lines **436**, ***with data/addresses passing on bus 90, 136***." '336, 17:34-37 (emphasis added). The buses **90** and **136** in Figure 17 are shown as ***bidirectional*** busses; i.e., the addresses and data therefore flow in ***both*** directions indicating that the CPU and I/O interface are "transmitting **and** receiving" that information.

TPL's argument that Plaintiffs' proposed construction would exclude an embodiment disclosed in the specification is misplaced because, as explained above, a bidirectional exchange is disclosed in the embodiment in Figure 17. It is well-known that a claim construction need not cover every embodiment disclosed in the specification. *See, e.g., Johns Hopkins Univ. v. CellPro*, 152 F.3d 1342, 1355 (Fed. Cir. 1998); *see also Boss Indus. v. Yamaha Motor Corp. U.S.*, No. 2:05-cv-422-DAK, 2007 U.S. Dist. LEXIS 98875, *12 (D. Utah Sept. 7, 2007). Because the term "exchanging" is clear and unambiguous, the Court must apply it as written without regard to

whether or not it would exclude disclosed embodiments. *See Lucent Techs., Inc. v. Gateway, Inc.*, 525 F.3d 1200, 1215-16 (Fed. Cir. 2008) ("[W]here we conclude that the claim language is unambiguous, we have construed the claims to exclude all disclosed embodiments.").

F. "As a function of parameter variation"

The '336 patent requires that the CPU's processing frequency and the clock rate of the on-chip *oscillator* vary in the same way "as a function of parameter variation" in fabrication or operational parameters, i.e., temperature, voltage and process. The parties' proposals are below:

Plaintiffs' Construction [JCCS 21]	**TPL's Construction**
in a determined **functional relationship** with parameter variation	Based on parameter variation

The specification explains that the temperature, voltage and process parameters in the environment "determine" the CPU's and the oscillator's frequencies in a "functional relationship:"

> The ring oscillator['s] frequency is ***determined by*** the parameters of temperature, voltage, and process. At room temperature, the frequency will be in the neighborhood of 100 MHZ. At 70 degrees Centigrade, the speed will be 50 MHZ. The ring oscillator **430** is useful as a system clock, . . . because its performance tracks the parameters which similarly affect all other transistors on the same silicon die.

'336, 16:59-67 (emphasis added.)

By disclosing that the ring oscillator's frequency is "determined by" the parameters and claiming that the CPU's processing frequency be a "function" of parameter variation, the claims require that the CPU's and the on-chip oscillator's frequencies have a specific and unique value for any given combination of temperature, voltage and process. Put another way, for a given combination of temperature, voltage and process parameters, the CPU's and the on-chip oscillator's frequencies should be reproducible.

Plaintiffs' proposed construction captures this requirement of a "determined" value. TPL's proposed construction is too vague, and leaves open the possibility, as environmental parameters vary, of non-reproducible, even random (i.e., undetermined) CPU and oscillator frequencies. Thus, TPL's proposal should be rejected. Plaintiffs' construction is consistent with and interpretive of the example quoted above, and should therefore be adopted.

G. "Originates from a source other than" ('336) and related terms

1. "a clock signal of said second clock originates from a source other than said ring oscillator variable speed system clock" ('336, claim 1)

Plaintiffs' Construction [JCCS 25]	**TPL's Construction**
a clock signal of said second clock is ***initially generated*** by a different source than said ring oscillator variable speed system clock	a clock signal of said second clock is ***generated*** by a different source than said ring oscillator variable speed system clock

2. a "a clock signal from said off-chip external clock originates from a source other than said oscillator" ('336, claim 6)

Plaintiffs' Construction [JCCS 26]	**TPL's Construction**
a clock signal of said off-chip external clock is ***initially generated*** by a different source than said oscillator	a clock signal of said off-chip external clock is ***generated*** by a different source than said oscillator

3. "a clock signal from said off-chip external clock originates from a source other than said variable speed clock" ('336, claim 10)

Plaintiffs' Construction [JCCS 27]	**TPL's Construction**
a clock signal of said off-chip external clock is ***initially generated*** by a different source than said variable speed clock	a clock signal of said off-chip external clock is ***generated*** by a different source than said variable speed clock

The three terms above were added during reexamination to distinguish over the Kato reference some ***two years <u>after</u>*** Judge Ward's claim construction order. Hence, the statements made by TPL to overcome the Kato reference should determine how these terms are construed.

TPL's proposed construction appears calculated to read the concept of "initially" out of the plain meaning of "originate:" It should be rejected as inconsistent with plain meaning. Plaintiffs' proposed construction, in contrast, is consistent with the plain meaning of "originate" and supported by the prosecution history during the reexamination, as explained below.

The disputed claim language was added during reexamination to overcome the Kato prior art, which discloses a first clock generating the "reference clock signal" for the second:

> **<u>Kato's clocks (14 and 15) were identified in the final Office action as corresponding respectively to the recited oscillator and the recited second (external) clock</u>**.[ ] However, Kato teaches at Col. 4, Lines 37-42:
>
> > The clock generating circuit comprises a first clock generator **14** and a second clock generator **15**. First clock generator **14** generates a **<u>reference clock</u>** signal ϕ0. Second clock **15** generator receives the **<u>reference clock</u>** signal ϕ0 from clock generator **14** and generates two clock signals ϕa and ϕb.
> >
> > . . .
>
> **<u>Clock signals ϕa and ϕb of second clock (15) clearly originate from clock generator (14), and in particular the clock signals ϕa and ϕb originate from clock signal ϕ0 of clock generator (14).</u>**

Amendment, 5/12/09, pp. 15-16 of 21, Chen Decl., Ex. K (emphasis added).

As admitted by TPL above, originating from a source means being initially generated by the source, in this case a reference clock. This definition is also consistent with the dictionary meaning of "originate—[t]o bring or come into being." *Webster's II New College Dictionary* at 773 (1995) (Chen Decl., Ex. Q). Hence, Plaintiffs' proposed construction should be adopted.

H. "(First) Push Down Stack," its connections ('336, '749 and '890) and related terms

Certain asserted claims in the '749 and '890 patents recite a "push down stack" having a "top item" and a "next item" connected to an arithmetic logic unit ("ALU"). One of the central concepts in these patents is the use of a ***first*** "push down stack" having both a "top item" and a "next item," both of which are directly coupled to an ALU.

The parties' competing constructions for "push down stack" are as follows:

Plaintiffs' Construction [JCCS 2]	**TPL's Construction**
a group of data storage elements organized **from top to bottom** to provide last-in first-out access to **stored** items, **wherein any previously stored items propagate towards the bottom by one data storage element while a new item is stored in the top data storage element**	Data storage elements organized to provide last-in first-out access to items

The term "push down stack" in computer science conventionally refers to a particular "last-in first-out" data storage structure. Its operation is often explained by analogy to a stack of plates on a spring-plate at a cafeteria. As with a cafeteria plate stack, the most recently stored (last-in) item sits at the top of the stack and is, therefore, the only item that is accessible (first-out). When a new plate is added to the stack, that new plate becomes the top item of the stack, thereby "pushing" the other plates down. The top item of the stack can be accessed (read) and/or removed from (or "popped off") the stack. When the top item is popped off, the second "plate" then becomes accessible as the new top item in the stack.

During prosecution of the '749 patent, the examiner complained that "the components . . . of the first push down stack as recited do not appear to render the push down stack to operate as a stack." '749, Office Action 12/31/92 (Chen Decl., Ex. R). The examiner went on to describe a push down stack as follows: "Note that a stack is such that inputted items ***propagate*** from one end of the stack to another via the stages in the stack." *Id.*

In response, the patent owner agreed with the examiner: "Thus, as the Examiner correctly

notes, these items [the connections to the ALU] do not render the first push down stack to operate as a stack. These items are in addition to the conventional construction of the first push down stack which allow it to operate as a stack." '749, Amendment 6/30/93 at 9 (Chen Decl., Ex. S). Hence, the construction of "push down stack" should include the "conventional construction" the examiner described: inputted items "propagate" from one end of the stack to the other.

As to other terms related to the "push down stack," as explained below, the specification expressly requires that the top and next items of the first push down stack be "directly coupled" to the ALU such that source and destination addresses are not used. The six disputed claim terms or phrases that implicate this issue, and the parties' competing positions, are set forth below:

1. "Push down stack **connected to** said arithmetic logic unit" ('749)

Plaintiffs' Construction [JCCS 1]	**TPL's Construction**
A push down stack comprising a top item register and a next item register, both **directly coupled to** the arithmetic logic unit **such that source and destination addresses are not used**	Ordinary meaning unless already defined – "push down stack," "connected to," "ALU"

2. "A top item **connected to** a first input of said arithmetic logic unit to provide the top item to the first input" ('749)

Plaintiffs' Construction [JCCS 9(a)]	**TPL's Construction**
A top item **directly coupled to** a first input of said arithmetic logic unit to provide the top item to the first input **such that source and destination addresses are not used**	Ordinary meaning, unless already defined - "arithmetic logic unit" and "connected to"

3. "A next item **connected to** a second input of said arithmetic logic unit to provide the next item to the second input" ('749)

Plaintiffs' Construction [JCCS 9(b)]	**TPL's Construction**
A next item **directly coupled to** a second input of said arithmetic logic unit to provide the next item to the second input **such that source and destination addresses are not used**	Ordinary meaning, unless already defined - "arithmetic logic unit" and "connected to"

4. "Push down stack with a top item register and a next item register, **connected to** provide inputs to the arithmetic logic unit" ('890)

Plaintiffs' Construction [JCCS 15]	**TPL's Construction**
push down stack comprising a top item register and a next item register, both **directly coupled to** inputs of the arithmetic logic unit **such that source and destination addresses are not used**	Ordinary meaning unless already defined – " push down stack," "connected to," "ALU"

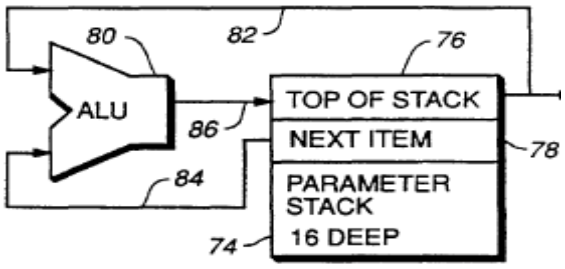
5. "ALU having an output **connected to** said means for storing a top item" ('749)

Plaintiffs' Construction [JCCS 3]	**TPL's Construction**
arithmetic logic unit having an output **directly coupled to** the top item register of the push down stack **such that source and destination addresses are not used**	Ordinary meaning unless already defined – "push down stack," "connected to," "ALU"

6. "An output of said arithmetic logic unit being connected **to** said top item register" ('890)

Plaintiffs' Construction [JCCS 16]	**TPL's Construction**
an output of the arithmetic logic unit being **directly coupled to** the top item register **such that source and destination addresses are not used**	Ordinary meaning unless already defined – "connected to," "ALU"

The requirement that the top item location and the next item location of the first push down stack be directly coupled to the ALU such that source and destination addresses are not used flows directly from the specification. These direct connections between the ALU and the push-down stack are shown in Figure 2 of the '749 patent (reproduced in relevant part below):



The ALU **80** shown in Figure 2 (above) has two inputs **82** and **84** for receiving data on which the ALU is to perform a logical or arithmetic operation and one output **86** on which the ALU provides the result of the operation. As can be seen from Figure 2, the two inputs come directly from the top item location **76** and next item location **78** of the push-down stack **74**, and the output **86** of the ALU is sent directly to the top item location **76** of the stack. '749, 6:29-34.

The specification describes the connections between the top and the next item locations of the push down stack and the ALU as "directly coupled:" "The microprocessor **50** architecture has **the ALU 80 (FIG.2) directly coupled to the top two stack locations 76 and 78**." '749, 19:6-8 (emphasis added). This direct coupling is not merely a feature of a preferred embodiment, but an essential aspect of the claimed invention.

The '749 patent explains that prior art microprocessors rely on instructions that not only specify the logical or arithmetic operation to be performed by the ALU, but must also include explicit addresses specifying the two "sources" of the data to be used and one "destination" to send

the result of the operation. '749, 26:68-27:3 ("Many 32-bit architectures use 8-bits to specify the operation to perform but use an additional 24-bits to specify two sources and a destination [because each of the three requires 8-bits for addressing].").

By having the ALU "directly coupled" to its two sources and one destination, their locations, i.e., "addresses," need not be explicitly specified in the instruction. As a result, instead of the 32-bit instruction of the prior art that requires 24-bits to explicitly specify the two sources and one destination for the ALU, the claimed microprocessor's instructions can be shortened to just 8-bits by eliminating the 24-bits used to explicitly identify the two sources and one destination. As explained in the '749 patent: "Most of the work in the microprocessor **50** is done by the 8-bit instructions . . . which are possible with the microprocessor because of the extensive use of implied stack addressing." '749, 25:65-68.

Resolving addresses takes extra instruction steps, extra bits in the instructions (for addresses) and time to execute the extra addressing steps. By directly coupling the top item location and the next item location of the push down stack to the inputs and output of the ALU, source and destination addresses need not be resolved, hence saving instruction steps, bits in the instructions, and time. The purported advantages of this technique over the prior art are repeatedly emphasized throughout the '749 patent:

- "The push down stack allows the use of **implied addresses**, **rather than the prior art technique of explicit addresses for two sources and a destination**." '749, 7:19-21.
- "Most microprocessors use on-chip registers for temporary storage of variables . . . A few microprocessors use an on-chip push down stack for temporary storage. A stack has the advantage of **faster operation compared to on-chip registers by avoiding the necessity to select source and destination registers.** (A math or logic operation always uses the top two stack items as source and the top of stack as destination.)" '749, 15:28-32.
- "For math and logic operations, the microprocessor 50 exploits the **inherent advantage** of a stack by **designating the source operand(s) as the top stack item and the next stack item**. The math or logic operation is performed, the operands are popped from the stack, and the result is pushed back on the stack. **The result is a very efficient utilization of instruction bits as well as registers**." '749, 26:4-11.
- "The availability of 8-bit instructions also allows another architectural innovation, the fetching of four instructions in a single 32-bit memory cycle." '749, 26:16-18.

By touting the use of implicit addressing and criticizing the prior art's use of explicit

addressing, the patent holder told the public that **not** using explicit addressing for the top and next item locations of the first push down stack was essential for the invention. Federal Circuit law is clear that "[w]hen the specification 'makes clear that the invention does not include a particular feature, that feature is deemed to be outside the reach of the claims of the patent, even though the language of the claims, read without reference to the specification, might be considered broad enough to encompass the feature in question.'" *Microsoft Corp.*, 357 F.3d at 1347 (quoting *SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys., Inc.*, 242 F.3d 1337, 1341 (Fed. Cir. 2001)).[8] Moreover, where, as here, the description of the invention "describes a feature of the invention ... and criticizes other products ... that lack that same feature, this operates as a clear disavowal of these other products...." *Edward Lifesciences LLC*, 582 F.3d at 1334; *see also, e.g.*, *Inpro II Licensing, S.A.R.L. v. T-Mobile USA, Inc.*, 450 F.3d 1350, 1354-56 (Fed. Cir. 2006) (narrowly construing claim to require a "direct connection" between components based on statements in specification touting performance advantages of such a connection).

During prosecution, the applicants also told the PTO that the claims' recited connections between the ALU and the top and next item locations of the first push down stack are "in addition to the conventional construction of the first push down stack . . . ." '749 File History, 6/30/93 Amendment at 9 (Chen Decl., Ex. S). The applicants emphasized the importance of the recited "additional" connections: "The [first push down] stack 74 in fact allows arithmetic operations to be carried out on operands supplied from it to the ALU and receives ALU results **as a result of the recited connections**.") *Id.* (emphasis added.)

TPL points to a "Return Stack 134" in Figure 2 to argue that the *first* push down stack is "addressable."[9] However, the return stack 134 is **not** the *first* push down stack claimed in the '749

[8] In *Microsoft Corp.*, for example, the Federal Circuit held that a claim covering a computer with a modem "connected to" a telephone line for "sending" and "receiving" information to a remote site required a direct, point-to-point connection between the two sites. 357 F.3d at 1347. While the claim language itself did not necessarily recite a direct point-to-point connection, the Court held that such an interpretation was the "inescapable conclusion" of the way the invention was described in the specification. *Id.* at 1348 ("Those statements, some of which are found in the 'Summary of the Invention' portion of the specification, are not limited to describing a preferred embodiment, but more broadly describe the overall inventions of all three patents.").

[9] TPL selectively quotes and mischaracterizes Dr. Wolfe's testimony. Dr. Wolfe testified that the

patent because it is not connected to the ALU. *See* Opening Brief, p. 8; *see also* Fig. 2 of '749. It is a completely separate stack, and is separately claimed as the "second push down stack" of claim 8, with different language reflecting its fundamentally different purpose and connections within the claimed microprocessor system. The distinction between the two stacks was emphasized during prosecution, too. '749, 6/30/93 Amendment at 9 ("The two stacks as now claimed serve distinct functions.") (Chen Decl., Ex. S).

In the context of the connections between the ALU and top and next items of the push down stack, therefore, "connected to" should be construed as "directly coupled . . . such that source and destination addresses are not used." The Court should also apply this definition to the use of "connected to" in the following two '749 means-plus-function claim elements:

7. (a) "means for storing a top item **connected to** a first input of said arithmetic logic unit to provide the top item to the first input"
   (b) "means for storing a next item **connected to** a second input of said arithmetic logic unit to provide the next item to the second input"

The parties have proposed the following definitions for these terms:

Plaintiffs' Construction [JCCS 8]	**TPL's Construction**
(a) Function: storing a top item connected to a first input of said arithmetic logic unit to provide the top item to the first input Structure: Top item register 76 of stack 74 **directly coupled** to a first input of ALU 80 through line 82 **such that source and destination addresses are not used.** (b) Function: storing a next item connected to a second input of said arithmetic logic unit to provide the next item to the second input Structure: Next item register 78 of stack 74 **directly coupled** to a first input of ALU 80 through line 84 **such that source and destination addresses are not used.**	Function: ***Ordinary meaning, unless defined elsewhere, including "arithmetic logic unit" and "connected to"*** Structure: ***register or its equivalents***

It is undisputed that these limitations are means-plus-function elements governed by 35 U.S.C. § 112 ¶ 6. Figure 2 (reproduced in relevant part above on p. 19 of this paper) illustrates the structure of the first push down stack and how it is connected to the ALU, and Plaintiffs' construction recites all the necessary structure disclosed in the specification. In contrast, TPL's identified structure equates a push down stack with a simple data register and fails to identify the

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push-down stack elements require implied addressing. Wolfe Depo. (Chen Decl., Ex. T) at 44:16-45:14. The Wolfe testimony TPL cites simply concerns what might or might not be considered "directly coupled." *Id.* at 79:8-80:9.

connections to the ALU that are central to the purported novelty of the invention.

The first step in construing a means-plus-function element is to identify the claimed function. *See Lockheed Martin Corp. v. Space Systems/Loral, Inc.*, 324 F.3d 1308, 1318 (Fed. Cir. 2003). The functions for these two means-plus-function claim elements are specified in the claim language itself, as reflected in Plaintiffs' proposed constructions. TPL's proposed construction, on the other hand, does not even attempt to identify the claimed function.

The second step is to identify the structure in the specification, if any, that performs the claimed function. *See Cardiac Pacemakers, Inc. v. St. Jude Med., Inc.*, 296 F.3d 1106, 1113 (Fed. Cir. 2002). Critically, "[a] structure disclosed in the specification qualifies as 'corresponding' structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim." *Default Proof Credit Card Sys., Inc. v. Home Depot U.S.A., Inc.*, 412 F.3d 1291, 1298 (Fed. Cir. 2005) (citing *B. Braun Med. Inc. v. Abbott Labs.*, 124 F.3d 1419, 1424 (Fed. Cir. 1997)).

Here, the only structures the specification "clearly links" to the function of storing a top item and a next item as recited in the claims are the top item register 76 and the next item register 78 of the push-down stack 74, respectively, directly coupled to the ALU as shown in Figure 2. These structures are reflected in Plaintiffs' proposed construction.

Under TPL's construction, however, any "register" could serve as one or both of the corresponding structures for these two claim elements. Under TPL's construction, for example, the corresponding structure for the means for storing a *top item* could be the *next item register* 78, or any other register, regardless of its structure or purpose. This would clearly be improper. TPL's construction improperly omits the clearly linked corresponding structure, including connections to other structures required to perform the claimed functions. Plaintiffs' construction should therefore be adopted.

I. "Connected to"

TPL has proposed a global construction of the phrase "connected to," to be applied throughout the patents-in-suit. TPL's intention is to read out of the claims the special connections that define the purported novelty of the "first push down stack" discussed above. The term

"connected to" appears in several of the asserted claims (claims 1, 6, 11 and 12 of '336, claims 1, 9, 18 and 23 of '749 and claims 1, 2 and 7 of '890). Because of the interactions of the "connected" components are different (e.g., the first push down stack's connections to the ALU are special), the meaning of "connected to" must depend on the context. Below are the parties' proposals.

Plaintiffs' Construction [JCCS 10]	**TPL's Construction**
The meaning of "connected to" depends upon how the connected components are supposed to interact.	"connected to" means "connected to convey signals to"

TPL's proposed construction does not construe "connected to" at all. Rather, it simply adds "convey signals to" after "connected to." Moreover, TPL's construction is so unreasonably broad and generic that it could be interpreted as meaning that two devices are "connected" if one device is able to convey signals to the other. *See* Opening Brief, p. 15 ("two components can be connected to convey signals without being directly connected"). If this was the case, essentially everything on the claimed microprocessor circuit would be "connected" to everything else.

TPL acknowledged the fallacy of this argument in the '336 reexamination. In an effort to overcome the Kato reference during reexamination of the '336 patent, TPL argued that such a broad construction of "connected" is "unreasonable:"

> An interpretation of the claim term 'connected' is unreasonable if the interpretation includes Kato's clock generator 14 connected to Kato['s] processing circuit . . . . An interpretation of the term 'connected' that leads to the conclusion that clock generator 14 is so connected leads to ***the unreasonable conclusion that every element [ ] in Kato's circuit is connected to every other element***. Such an interpretation of the term 'connected' obviates both the meaning and use of the term in Claim 1 because every element of the claimed circuit of Claim 1 would be connected under this interpretation.

Amendment, 9/8/08, p. 23 of 28, Chen Decl., Ex. P (emphasis added).

TPL's unreasonably broad construction should be rejected. The term "connected to" must be construed based upon the interactions between the components to be "connected," the specific context of the specific claim language, and how it is described in the specification. *Epcon Gas Sys., Inc. v. Bauer Compressors, Inc.*, 279 F.3d 1022, 1031 (Fed. Cir. 2002) (construing the term "substantially" differently in the same claim in the context of language of approximation – "substantially constant" —versus language of magnitude—"substantially below"); *see also Microprocessor Enhancement Corp. v. Tex. Instruments Inc.*, 520 F.3d 1367, 1375 (Fed. Cir.

2008) (the controlling factor for whether multiple appearances of a term should be consistently construed is the **context in which each term appears**).

J. "Means for fetching instructions" ('749 and '890) and related terms

1. "supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle"

This phrase appears in claims 1 and 8 of the '749 patent, as a part of a larger phrase defining the capabilities of the claimed means for fetching instructions. *See* '749, claim 1 ("said means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and **supply the multiple sequential instructions to said central processing unit during a single memory cycle**."). The parties have proposed the following constructions for this phrase (boldface type showing differences):

Plaintiffs' Construction [JCCS 5]	**TPL's Construction**
Provide the multiple sequential instructions in parallel **(as opposed to one-by-one)** to said central processing unit integrated circuit during a single memory cycle **without using a prefetch buffer or a one-instruction-wide instruction buffer, that supplies one instruction at a time**	Provide the multiple sequential instructions in parallel to said central processing unit integrated circuit during a single memory cycle

The additional language in Plaintiffs' proposed construction comes directly from TPL's express disclaimer made during reexamination in which it attempted to distinguish U.S. Patent No. 4,680,698 to Edwards (Chen Decl., Ex. U):

> Edwards describes the way the Transputer decodes and executes instructions. ***As described in Edwards,*** see, e.g., Fig. 8, below, ***instructions are supplied to a one-instruction-wide instruction buffer, one at a time***, and are there decoded. ***Fetching multiple instructions into a prefetch buffer and then supplying them one at a time is not sufficient to meet the claim limitation*** – the supplying of 'multiple sequential instructions to a CPU during a single memory cycle.'

Amendment, 1/19/10, p. 26 of 58, Chen Decl., Ex. V (emphasis added).

It is hard to imagine a more clear and unmistakable disclaimer than the one TPL provided above, in which TPL told the PTO that the requirement of claims 1 and 8, supplying multiple sequential instructions to a CPU during a single memory cycle, is **not** satisfied by using a pre-fetch buffer or a one-instruction wide buffer (as disclosed in Edwards) that supplies one instruction at a time. TPL is bound to such admission, which should be incorporated into the Court's construction of this phrase. *See, e.g., Rheox, Inc.*, 276 F.3d at 1325 ("Explicit arguments made during

prosecution to overcome prior art can lead to narrow claim interpretations because 'the public has a right to rely on such definitive statements made during prosecution.'") (citations omitted); *see also Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1324 (Fed. Cir. 2003) ("where the patentee has unequivocally disavowed a certain meaning to obtain his patent, the doctrine of prosecution disclaimer attaches and narrows the ordinary meaning of the claim congruent with the scope of the surrender"). TPL even admits that "the patent teaches the feature of being able to fetch and supply multiple instructions in parallel in a single cycle ***without using an intervening prefetch buffer***," which supports Plaintiffs' proposal. Opening Brief, p. 12 (emphasis added). Plaintiffs' proposed construction should therefore be adopted.

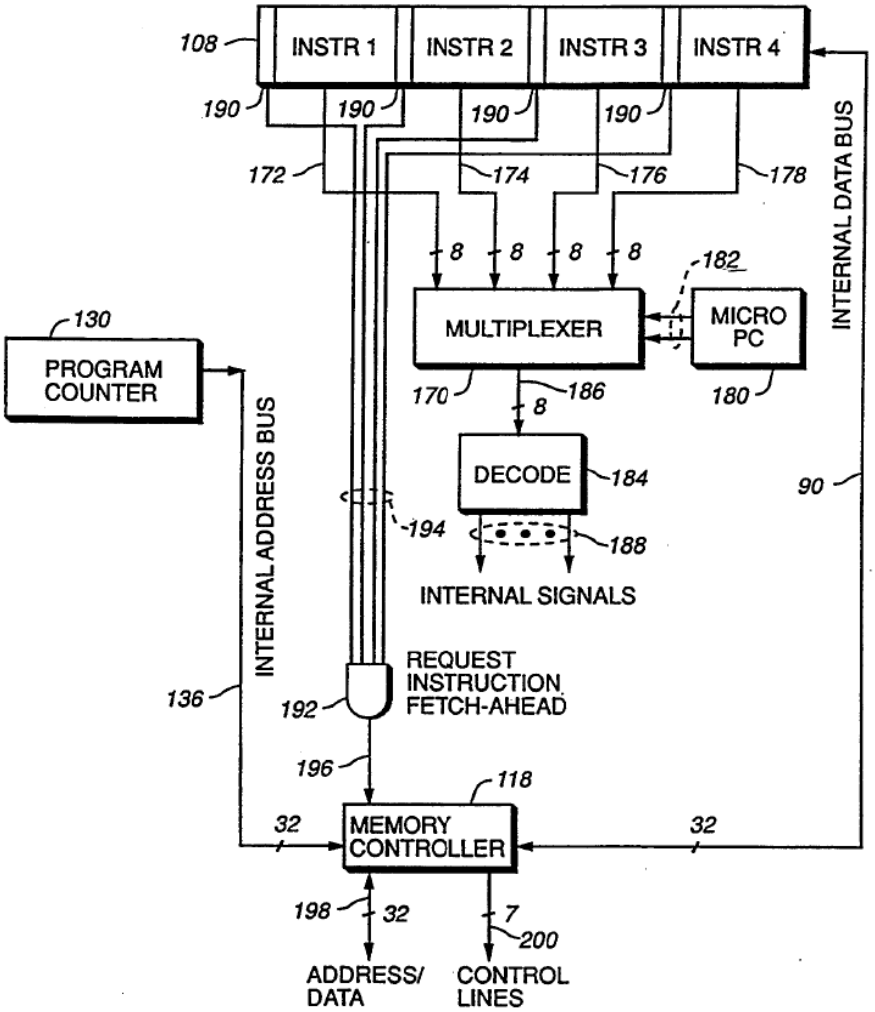
2. "means connected to said bus for fetching instructions for said central processing unit integrated circuit on said bus from said memory, said means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle"

Plaintiffs' Construction [JCCS 4]	**TPL's Construction**
Function: fetching instructions for said central processing unit integrated circuit on said bus from said memory, being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle Corresponding § 112 ¶6 structure (Fig. 4): Memory controller 118 connected to instruction register 108 through internal data bus 90 and, to program counter 130 through internal address bus 136, ***and to Request Instruction Fetch-Ahead 192 via line 196, and Request Instruction Fetch-Ahead 192 is connected to instruction register 108 via lines 194.***	Function: fetching instructions for said central processing unit integrated circuit on said bus from said memory, being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle, ***wherein the fetched "multiple sequential instructions" are supplied to the instruction register 108 during the same memory cycle they are fetched.*** Corresponding § 112 ¶6 structure: Memory controller (118) Instruction register (108) Internal data bus (90) Program counter (130) Internal address bus (136)

With respect to the claimed function, Plaintiff's proposed construction comes directly from the language of the means-plus-function claim element. TPL's construction, on the other hand, adds an extraneous "wherein" clause that is not part of the claim and, therefore, not part of the recited claim function. TPL's failure to properly identify the claimed function – the threshold determination in construing a means-plus-function element – mandates rejection of its proposal.

With respect to the corresponding structure, the parties do not dispute that the structure includes at least the program counter **130**, the internal address bus **136**, the memory controller **118**, the instruction register **108** and the internal data bus **90**, as shown in Figure 4 of the '749 patent (reproduced below). The main dispute is whether the required structure also includes the ***request instruction fetch-ahead 192*** and its connecting buses, **194** and **196**, as Plaintiffs have proposed.

As discussed above, the specification of '749 states that "[t]he availability of 8-bit instructions also allows another architectural innovation, the fetching of four instructions in a single 32-bit memory cycle." '749, 26:16-18. Here, this feature is expressly claimed in the means-plus-function element: "means for fetching instructions being configured and connected to ***fetch multiple sequential instructions from said memory in parallel*** and supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle," whose structure is shown in Figure 4 of '749 below:



The request instruction fetch-ahead **192** in Figure 4 is part of the corresponding structure because the claimed "means for ***fetching instructions*** being configured and connected to fetch multiple sequential instructions from said memory ***in parallel***" is described as including the instruction fetch-ahead. As disclosed by the specification, "[t]he approach of this microprocessor to speed is to ***overlap*** *instruction fetching with execution of the previously fetched instruction(s).*" '749, 21:30-33 (emphasis added.) The request instruction fetch-ahead **192** is the only structure in Figure 4 that requests "instruction fetching" from memory that is overlapping (or "in parallel") with "execution of previously fetched instruction(s)." *Id.*

The request instruction fetch-ahead **192** requests a "parallel" fetch only when none of the current set of instructions requires memory access. '749, 8:4-7. The reason is that if any of the current set of instructions requires memory access, then any instructions, if fetched "in parallel," would have to be discarded in favor of the memory access required by the ***current*** set of instructions. This feature of the request instruction fetch-ahead **192** is explained below:

> In operation, ***when*** the most significant bits **190** of remaining instructions **1-4** are '1' in a clock cycle of the microprocessor **50**, ***there are no memory reference instructions in the queue***. The output of ***[request instruction fetch-ahead] 192 on line 196 requests an instruction fetch ahead by memory controller 118 without interference with other accesses***. ***While the current instructions in instruction register 108 are executing, the memory controller 118 obtains the address of the next set of four instructions from program counter 130 and obtains that set of instructions.*** By the time the current set of instructions has completed execution, the next set of instructions is ready for loading into the instruction register.

'749, 8:4-16.

As explained above, bits **190** (*see* Figure 4, reproduced on p. 27 of this paper) of the current set of instructions in the instruction register **108** indicate whether they require memory accesses. When bits **190** are all "1," "there are no memory reference instructions" that require memory accesses. *See id*. Hence, the instruction fetch-ahead **192** can make a request for fetching "in parallel" the next set of instructions to the memory controller **118** "without interference with other accesses" otherwise needed by the current set of instructions. In response to such request, "the memory controller **118** obtains the address of the next set of four instructions from program counter **130** and obtains that set of instructions." '749, 8:10-13.

Even TPL's Opening Brief acknowledges that the claimed "parallel" fetch requires that the next set of instructions be fetched ahead, while the current set of instructions is being executed by the CPU: "TPL's proposed function emphasizes that the **parallel** fetch brings the instruction from memory to the instruction register of the of the CPU in the requisite single memory cycle. **By the time the current set of instructions has completed execution, the next set of instructions is ready for loading into the instruction register.**" Opening Brief, p. 23 (emphasis added) (citation omitted). As discussed, the instruction fetch-ahead **192** is the only disclosed structure that requests such "**parallel** fetch," and hence must be included to perform the claimed function.

Furthermore, the Federal Circuit's ruling in *Asyst Technologies, Inc. v. Empak, Inc*., 268 F.3d 1364, 1372 (Fed. Cir. 2001) dictates that all components connecting required components in the corresponding structure for a means-plus function element must also be included as part of the corresponding structure. The *Asyst* Court found that the corresponding structure of the "fourth means" includes the local process controller, the communication means, and "***necessarily includes [the] structure that connects the two***, i.e., [the] communication line." *Id*. (emphasis added).

Here, the request instruction fetch-ahead decoder **192** and its connecting buses **194** and **196** in Figure 4 of the '794 patent (reproduced on p. 27 of this paper) connect two required components, the instruction register **108** and the memory controller **118**, as admitted by TPL. *See* Opening Brief at pp. 22, 24. Hence, the request instruction fetch-ahead decoder **192** and its connecting buses **194** and **196** are directly analogous to the communication line connecting two required components in *Asyst*, so they must be included as part of the corresponding structure.

As discussed above, the request instruction fetch-ahead **192** is required because it is the ***only*** disclosed component that requests from memory an overlapping instruction fetch[10] in parallel "[w]hile the current instructions in instruction register **108** are executing." '749, 8:7-13. The

[10] Even TPL admits that when no memory accesses are needed by the current set of instructions ('749, 8:4-7), "a fetch is requested ahead of instruction execution [by the request instruction fetch-ahead **192**]." Opening Brief, p. 24. However, there is no support that "otherwise a fetch is requested once all instructions in the instruction register have executed[,]" as claimed by TPL. *See id*. TPL cites no support in the specification as to what component makes such fetch request in this situation, and nor can TPL because there is none in the specification.

request instruction fetch-ahead **192** and its connecting buses **194** and **196** also connect two required components, the instruction register **108** and the memory controller **118**, as admitted by TPL. Hence, they must be part of the corresponding structure for the claimed "means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory ***in parallel***," and consequently Plaintiffs' proposed structure should be adopted.

K. "Instruction register" ('749 and '890) and related terms

Plaintiffs' Construction [JCCS 12]	**TPL's Construction**
register that receives and holds one or more instructions for supplying to circuits that interpret the instructions**, in which any operands that are present must be right-justified in the register**	register that receives and holds one or more instructions for supplying to circuits that interpret the instruction

The dispute here is whether any "operands" must be "right justified" in the "instruction register." The same issue was fully litigated by TPL in the prior Texas case before Judge Ward, *TPL v. Matsushita*, Case No. 2:05-cv-494. As explained below, TPL lost this issue before Judge Ward and stipulated to a judgment of non-infringement, and that judgment is now final.

The '749 patent has a division, U.S. Patent No. 5,784,584 ("'584 patent"), which claims features of the same structure in Figure 4 (on the cover page of '584) that supports the disputed term here, "means for fetching instructions," as admitted by TPL. *See* Opening Brief, p. 24 ("Figure 4 shows . . . the corresponding structure for the fetching means."). The '584 patent was a subject of the prior litigation, and originally part of this action, too, until TPL granted a covenant-not-to-sue to the Plaintiffs. *See, e.g.*, Dkt. 152, p. 2, *HTC v. TPL*, 5:08-cv-882.

In the prior litigation, a hotly contested issue was whether any "operands" in the "instruction register" (depicted as 108 in Figure 4) must be "right justified." There, TPL similarly contended that "right justified operands are a feature of the preferred embodiment." Ward Order (Chen Decl., Ex. A), p. 22. Judge Ward rejected TPL's contention, and ruled that "[t]he specification and prosecution history refer to the fact that ***operands in the instruction register must be right justified***." *Id.* at 23 (emphasis added). TPL then stipulated to a judgment of non-infringement as a result, and appealed this issue to the Federal Circuit, again arguing that right-justified operands are nothing but a feature of the preferred embodiment. *See* TPL Appeal Brief, p. 25 (Chen Decl., Ex. W). The Federal Circuit rejected TPL's arguments and summarily affirmed

Judge Ward's decision. *See* Fed. Cir. Ruling (Chen Decl., Ex. X). Hence, this issue is settled as a matter of law, and collateral estoppel applies.

It is no wonder that TPL consistently lost this issue before Judge Ward and the Federal Circuit given the clear and unmistakable disclosures in the '749 and '584 patents. As admitted by TPL in its Opening Brief, during prosecution of the '749 patent, the applicants argued to the PTO that the feature of having operands "right justified" distinguished over the Boufarah prior-art reference as to the claim that became claim 1 of the '749 patent. Opening Brief, p. 11, n. 8. In subsequent reexaminations of the '584 patent, a division of '749, TPL repeatedly pointed to the "right-justified" operands in the instruction register to overcome prior art (*see* Chen Decl., ¶ 26, Ex. Y), which is disclosed in the specification as follows:

> This magic is possible because ***operands must be right justified in the instruction register***. This means that the least significant bit of the operand is always located in the least significant [i.e., right-most] bit of the instruction register.

'749, 18:44-47 (emphasis added).

Note that the quoted section above is what Judge Ward relied upon in ruling that "[t]he specification and prosecution history refer to the fact that ***operands in the instruction register must be right justified***." Ward Order (Chen Decl., Ex. A), p. 23 (emphasis added).

TPL argues that only "variable width operands must be right justified in the instruction register." Opening Brief, p. 11. However, there is no disclosure in the specification of any "fixed width" operand that does not have to be right-justified, as TPL contends. *Id.* The so-called example (and the citation of '749, 31:35-32:16, entitled "Handling On-Chip Variables") provided by TPL shows no "operands" that are not right-justified. The cited section describes the handling of on-chip variables in connection with the Return Stack **134**, which does not even appear in Figure 4 (reproduced on p. 27 of this paper) that provides the corresponding structure for the "means for fetching instructions." In fact, the term "operand" does not appear at all in the section cited by TPL, let alone anything discussing whether it is "fixed width" or "right justified." Hence, the section cited by TPL is irrelevant to the dispute here.

TPL does not, and cannot, cite a single instance of any operand in the specification that is **not** right justified, as shown by ARM, Inc. (TPL's opponent in the Texas litigation) and agreed by

the Federal Circuit. *See* ARM Appeal Brief, pp. 23-24 (Chen Decl., Ex. Z) ("**The Specification Confirms The Right Justified Operands Are the Only Embodiment Described.**") (boldface and underlining in original). TPL's argument hence should be rejected (as was it repeatedly by Judge Ward and the Federal Circuit), and Plaintiffs' proposed construction should be adopted.

For the same reasons above, Plaintiffs' constructions below should be adopted:

1. "multiple sequential instructions" ('749, '890)

Plaintiffs' Construction [JCCS 7]	**TPL's Construction**
Two or more instructions in sequence, **in which any operands that are present must be right-justified in the instruction register**	Two or more instructions in a program sequence

2. "sequence of program instructions" ('148)

Plaintiffs' Construction [JCCS 30]	**TPL's Construction**
Two or more instructions in sequence, **in which any operands that are present must be right-justified in the instruction register**	One or more instructions in a program sequence

As noted above, Judge Ward previously ruled that operands must be right justified in the instruction register, which caused him to construe "instruction groups," a claim term in the '584 patent, to incorporate this requirement. *See* Ward Order (Chen Decl., Ex. A), p. 8. He accordingly construed "instruction groups" as "sets of from 1 to a maximum number of ***sequential instructions***, each set being provided to the ***instruction register*** as a unit and having a boundary, and in which ***any operand that is present must be right justified***." *Id.* (emphasis added).

The disputed term here, "multiple sequential instructions," should be simply construed as "two or more instructions in sequence, in which any operands that are present must be right-justified in the instruction register" as proposed by Plaintiffs. The term "sequence of program instructions" should be construed the same way as Plaintiffs have proposed.

TPL's construction of "sequence of program instructions" is flawed because it would cover a single instruction ("**one** or more instructions"), which is contrary to the plain meaning of the term "instruction**s**" in its plural form. TPL's constructions also fail to incorporate the right justified operand feature that, as explained above, is essential to the claimed invention. Hence, TPL's proposal should be rejected, and Plaintiffs' proposal should adopted in its entirety.

L. "Central processing unit" and related terms ('890)

The parties stipulated to Judge Ward's construction of "central processing unit" from the

prior litigation, which is "an electronic circuit on an integrated circuit that controls the interpretation and execution of programmed instructions." The parties currently dispute two terms from the '890 patent, "main central processing unit" and "separate direct memory access central processing unit," which are recited in claim 1 of the '890 patent as a complementary pair. *See* '890 patent, claim 1 ("A microprocessor, which comprises a **main central processing unit** and a **separate direct memory access central processing unit** in a single integrated circuit comprising said microprocessor . . ."). The parties have proposed the following constructions:

1. "main central processing unit" ('890)

Plaintiffs' Construction [JCCS 11]	**TPL's Construction**
A principal central processing unit that does not perform direct memory access related operations	A main electronic circuit on an integrated circuit that controls the interpretation and execution of programmed instructions

2. "separate direct memory access central processing unit" ('890)

Plaintiffs' Construction [JCCS 14]	**TPL's Construction**
A separate central processing unit that fetches and executes instructions for performing direct memory access without using the main central processing unit	Electrical circuit for reading and writing to memory that is separate from a main CPU

Claim 1 of the '890 patent makes clear that "main central processing unit" (main CPU) and the "separate direct memory access central processing unit" (separate DMA CPU) are distinct components that serve different but complementary purposes. The specification is explicit that the purpose of the DMA CPU is to relieve the main CPU of the burden of performing direct memory access functions. The terms should be construed consistently with that functionality.[11]

As explained below, the claims recite a "DMA CPU," and the specification distinguishes a DMA CPU from a "DMA controller." Given that distinction, it is improper to construe the claim term "DMA CPU" as somehow including a "DMA controller." If the patentee intended the claims to include a DMA controller, the term "DMA CPU" should not have been used.

The specification of the '890 criticizes "conventional microprocessors" that use "DMA

[11] TPL mischaracterizes the testimony of Dr. Wolfe on this point. When asked if the main CPU can perform any DMA-related operations, he testified: "Any? I don't think so." Wolfe Depo. (Chen Decl., Ex. T.) at 167:11-12. Dr. Wolfe did say that the main CPU can request a single element of data from memory, but made clear that is not a "DMA-related" function. Wolfe Depo. (Chen Decl., Ex. T) at 167:19-168:10.

controllers" because "**some processing by the main central processing unit (CPU) of the microprocessor is required**." '890, 1:52-58 (emphasis added).

The specification of the '890 patent purports to address this deficiency by disclosing a feature unavailable in conventional microprocessors using DMA controllers:

> It is a further ***object of the invention*** to provide a high performance microprocessor in which ***DMA does not require use of the main CPU during DMA requests and responses and which provides very rapid DMA response with predictable response times***.

'890, 2:1-5 (emphasis added).

This objective is accomplished through a separate DMA CPU:

> The DMA CPU **72** ***controls itself*** and ***has the ability to fetch and execute instructions***. It operates as a co-processor to the main CPU **70** (FIG. 2) for time specific processing.

'890, 8:22-24 (emphasis added).

TPL concedes in its Opening Brief that "DMA controllers" are different from the claimed "DMA CPU:" "This 'more traditional DMA controller' is one that functions more as a traditional state machine, ***without the ability to fetch its own instructions that characterizes a CPU***." Opening Brief, p. 15:10-12 (emphasis added). Having admitted that a DMA controller is different from a DMA CPU, and that it is "the ability to fetch its own instructions that characterizes a CPU," *id.*, there is no basis for TPL to argue that the "DMA **CPU**" need not have the ability to fetch its own instructions. TPL's attempt to read the "**CPU**" limitation out of the phrase "DMA **CPU**" should be rejected, and Plaintiffs' construction should therefore be adopted.

TPL relies solely upon the fact that Figure 9, "a layout diagram of a second embodiment of a microprocessor" ('890, 4:61-62), shows a "DMA CPU **314**," while the text of the specification describes separately **another embodiment** in which "the DMA processor **72** of the microprocessor **50** has been replaced with a more traditional DMA controller **314** . . ." '890, 12:62-13:4. This passage, however, does ***not*** refer to Figure 9 at all. In fact, nowhere in the specification is Figure 9 described as including a "DMA controller."

TPL mischaracterizes the specification as somehow equating the DMA CPU **314** of Figure 9 with a DMA controller. The correct reading is that the specification describes **two separate**

embodiments: one illustrated in Figure 9 as including a "DMA CPU 314," and another one described in the specification (but not illustrated) where the "DMA processor" is replaced with a "DMA controller." TPL's proposal hence should be rejected.

M. "multiplexing means on said bus between said central processing unit and said dynamic random access memory, said multiplexing means being connected and configured to provide multiplexed row addresses, column addresses and data on said bus from said central processing unit to said dynamic random access memory and to provide data from said dynamic random access memory to said central processing unit" ('749)

Plaintiffs' Construction [JCCS 6]	**TPL's Construction**
Function: being connected and configured to provide multiplexed row addresses, column addresses and data on said bus from said central processing unit to said dynamic random access memory and to provide data from said dynamic random access memory to said central processing unit. Corresponding § 112 ¶6 structure (Fig. 12): (1) MUX 378 connected to MUX 382 **through MUXED ADDRESS BUS 380**; (2) MUX 378 connected to the unnumbered MUX between MUX 378 and MUX 382 **via the two unnumbered MUXED ADDRESS BUSES (labeled "$A_{23} – A_{13}$" and "$A_{12} – A_2$," respectively) between MUX 378 and such unnumbered MUX** (3) MUX 382 connected to the unnumbered MUX between MUX 378 and MUX 382 **via the two unnumbered MUXED ADDRESS BUSES (labeled "$A_{23} – A_{13}$" and "$A_{12} – A_2$," respectively) between MUX 382 and such unnumbered MUX**	Function: providing data, column addresses, row addresses to a bus, wherein row addresses and column addresses and data can be provided to the bus at different times. Corresponding § 112 ¶6 Structure: MUX (382); MUX (378); and MUX in Fig. 12 between 382 and 378

TPL does not dispute that Figure 12 in the '890 patent supports this term. However, TPL seeks to exclude the buses (labeled as "$A_{23} – A_{13}$" and "$A_{12} – A_2$.") connecting the three multiplexers (labeled as MUX 382, MUX 378 and an unnumbered MUX in the middle) that the parties have agreed are part of the required structure. However, the required structure "necessarily includes" components connecting other required components, so the connecting buses must be included. *Asyst*, 268 F.3d at 1372. Hence, Plaintiffs' proposed structure including such buses (labeled as "$A_{23} – A_{13}$" and "$A_{12} – A_2$.") should be adopted.

TPL's proposed function is not supported by the intrinsic record, and hence should be rejected. Plaintiffs' proposed function should be adopted and construed under plain meaning.

III. CONCLUSION

For the foregoing reasons, Plaintiffs' constructions should be adopted in their entirety.

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ATTESTATION PER GENERAL ORDER 45

I, Kyle D. Chen, am the ECF User whose ID and password are being used to file Plaintiffs' Consolidated Responsive Claim Construction Brief. In compliance with General Order 45, X.B., I hereby attest that the counsel listed above have concurred with this filing.

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